Amendments to the Claims:

This Listing of Claims, as below, will replace all prior versions of claims in the present application:

Listing of Claims:

1. (Cancelled).

2. (Canceled)

3. (Cancelled).

4. (Cancelled).

5. (Cancelled)

6. (Cancelled).

7. (Cancelled).

8. (Cancelled).

9. (Cancelled).

10. (Cancelled).

11. (Cancelled).

12. (Cancelled).

13. (Currently amended) A method comprising:

monitoring trends of phase adjusts of signals from a phase rotator control of a clock-data-recovery circuit to a reference clock of a serial receiver, including utilizing an up-down counter and an adder to accumulate phase adjust data from the phase adjusts, wherein the phase adjusts include first rotate up and rotate down signals for phase rotation in the clock-data-recovery circuit; and

adapting the phase adjusts to create future adjusts based on previous adjusts, including utilizing combinatorial logic to generate the future adjusts based on the accumulated phase adjust data and the previous adjusts, wherein the future adjusts include second rotate up and rotate down signals improving a rate of compensation for the frequency offsets by the phase adjusts, and wherein the first rotate up and rotate down signals and the second rotate up and rotate down signals are logically ORed to provide the phase adjusts to the reference clock.

14. (Cancelled).

15. (Cancelled).

16. (Currently amended) The method of claim [[15]] 13 ~~wherein the phase adjusts further comprise rotate up and rotate down signals for phase rotation in the clock-data recovery circuit, and~~ wherein utilizing the combinatorial logic includes generating ~~a new~~ the second rotate up signal based on an overflow in the adder.

17. (Currently amended) The method ~~circuit~~ of claim 16 wherein utilizing the combinatorial logic includes generating ~~a new~~ the second rotate down signal based on an underflow in the adder.

18. (Currently amended) The method ~~circuit~~ of claim [[14]] 13 ~~wherein the phase adjusts further comprise rotate up and rotate down signals for phase rotation in the clock-data recovery circuit, and~~ wherein the adder accumulates a chosen number of most significant bits of the up-down counter ~~rotate up and rotate down signals~~.

19. (Cancelled).

20. (Cancelled).

21. (Cancelled).

22. (Cancelled).

23. (Cancelled)

24. (New) A method comprising:

generating first rotate up and rotate down signals for phase adjusts in a receiver link to adapt to frequency offsets, the first rotate up and rotate down signals causing rotation of a phase of a clock signal up or down to compensate for the frequency offsets; and

detecting trends in the first rotate up and rotate down signals using an adjust circuit, and using combinatorial logic to adapt the first rotate up and rotate down signals for the phase adjusts based on accumulated data accumulated by an adder by generating second rotate up and rotate down signals improving a rate of compensation for the frequency offsets by the phase adjusts, the improvement relative to the compensation provided by using only the first rotate up and rotate down signals for adapting to the frequency offsets, and wherein the first rotate up and rotate down signals and the second rotate up and rotate down signals are logically ORed to provide the phase adjusts of the clock signal.

25. (New) The method of claim 24 wherein the detecting trends includes monitoring for an overflow of the first rotate up and rotate down signals.

26. (New) The method of claim 25 wherein the detecting trends includes monitoring for an overflow by counting and accumulating the first rotate up and rotate down signals.

27. (New) The method of claim 25 wherein the detecting trends includes monitoring for an overflow with an up/down counter coupled to the adder.

28. (New) The method of claim 27 wherein the generating of the second rotate up and rotate down signals includes detection of overflow and underflow in the adder and logically combining the overflow and underflow with the first rotate up and rotate down signals by the combinatorial logic.

29. (New) A method comprising:

using an up/down counter for counting rotate up and rotate down signals from a phase rotator control for phase adjustments by a clock-data-recovery loop of a serial receiver;

using an adder coupled to the up/down counter that outputs accumulated data indicative of a trend in the phase adjustments; and

using combinatorial logic coupled to the adder to adapt the rotate up and rotate down signals based on the accumulated data, wherein the combinatorial logic generates a new rotate up signal based on an overflow in the adder and wherein the combinatorial logic generates a new rotate down signal based on an underflow in the adder.

30. (New) The method of claim 29 wherein the adder accumulates a chosen number of most significant bits of the up/down counter.

31. (New) The method of claim 29 wherein the rotate up and rotate down signals are for phase adjusts in a receiver link to adapt to frequency offsets and causing rotation of a phase of a clock signal up or down to compensate for the frequency offsets, and wherein the new rotate up and rotate down signals improve a rate of compensation for the frequency offsets by the phase adjusts, the improvement relative to the compensation provided by using only the rotate up and rotate down signals for adapting to the frequency offsets, and wherein the rotate up and rotate down signals and the new rotate up and rotate down signals are logically ORed to provide the phase adjusts.